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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/070,313 | 03/05/2002 | Masayuki Ito | TAMA.0003 | 2895 |

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| EXAMINER | |
|---|---|
| THOMAS, SHANE M | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2186 | 6 |

DATE MAILED: 11/19/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/070,313 | ITO ET AL. | |
| | Examiner | Art Unit | |
| | Shane M Thomas | 2186 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) 1-14 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-14 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 16 Novemeber 1999 is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. §§ 119 and 120**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2 & 5.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

## DETAILED ACTION

### *Drawings*

Figures 9A, 9B, 9C, and 9D should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

### *Claim Objections*

Claims 1-14 are objected to because of the following informalities:

As per claims 1, 5, and 9, the examiner recommends amending the phrase --so as to locate the data-- to --so as to *arrange* the data-- such as stated in claim 4. --Locating-- data in order of addresses does not positively recite correct operation of a fill operation.

As per claims 4 and 5 the claims do not specifically state that --L times one over two to the n-th power-- is the burst length. Therefore, the examiner recommends amending the claims to read, --where L times one over two to the n-th power *is the range*, and the burst length is allowed ... --.

As per claims 7 and 13, line 3, --axquired-- should be corrected to --acquired--. Regarding line 6, --meat-- should be corrected to --meant--.

As per claims 2,3,6, and 10-12, they are dependent on objected claims.

***Claim Rejections - 35 USC § 112***

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 4-8 and 12-14 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claims 4 and 5, it is not clear to the examiner whether the applicant is defining a--natural number-- as including zero. Webster's Collegiate Dictionary defines a --natural number-- as a positive integer. In the disclosure, the applicant states that the burst length can be equal to the cache line length. For this to be true, the variable 'n' of the --equation-- of the burst length in the claims, must be equal to zero. As the claims read currently, if 'n' is equal to one, the largest burst length would be "L/2" or one-half the cache line size, which contradicts the disclosure. The examiner recommends amending the claims, replacing --natural number-- with --an integer greater than or equal to zero-- or the like. The examiner will examine the claims with regard to the recommended amendment.

As per claims 6-8 and 12-13, they are rejected as being dependant upon rejected claims 4 and 5.

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 4,5, and 9 are rejected under 35 U.S.C. 102(b) as being anticipated by Kundu et al. (U.S Patent No. 5,715,476).

As per claims 1, 4, 5 and 9, Kundu shows a data processing system in figure 1 comprising a CPU 101, a cache 104, and a memory control 108 accessible to a memory 109. The examiner is considering the cache control part to be comprised in the cache 104. Further the examiner is considering the combination of the processor 101, the cache 104, and the memory control 108 to be a --data processing device--. The main memory 109 is comprised of a plurality of memories (SDRAM modules) 201-203 as shown in figure 2. --First information-- for indicating a burst length is contained in register 212 in the cache/memory control 108, more specifically in the smart increment control logic 117. The burst length is also stored in the mode registers 201A-203A of the SDRAM modules (column 8, lines 13-14). The burst length of the memory device can be divisible by consecutive powers of 2, thus yielding a burst length range of 1,2,4,or 8 words as described in column 5, lines 38-40.

Figure 3 shows the data addresses associated with different burst lengths. Because the burst length is configurable (column 5, lines 38-39) and a cache line is a constant size, single or multiple bursts are required to fill a cache line. The examiner is

considering a single burst operation to fill the cache line according to figures 3A-3C. As can be seen by the figures, the starting address of the cache miss is the starting address of the data arrangement. For example, in figure 3C, if the 4th block in the cache line is the result of a cache miss (mishit), and the fill line returns with the 4th block of the line. Data following the address of the miss in the line fill are arranged in linear order. The address of the 5th block comes after the 4th block and so on. In addition, if the starting block address (cache miss address) is not the beginning block of the cache line (block address 0), the address --wraps-around-- when being fetched from memory. The first block address (address 0) is arranged after the last block address in the cache line (address 7) as seen in figure 3C.

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2,6,7,10,12,13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kunda et al. (U.S. Patent No. 5,715,476) in view of Gaskins et al. (U.S. Patent No. 6,081,853).

As discussed above in the rejection for claims 1,4,5, and 9, Kunda shows a cache in the data processing device of figure 1; however, specific detail of the cache and its interaction with the memory, as are well know in that art, are not discussed in detail.

Therefore the examiner is incorporating the cache system shown in figure 2 of Gaskins to further illustrate the cache memory 104 of Kunda. It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the cache of the data processing device of Kunda with the cache memory shown in figure 2 of Gaskins because the cache memory of Gaskins is a prior art cache for use with burst operations from a main memory (refer to column 4, lines 36-37 of Gaskins). Figures 2 and 3 and column 8, lines 18-28, of Gaskins refer to the common operation of a cache miss and line fill operation. Address information is sent to the memory on where to fetch the data. The cache memory 104 (figure 1) of Kunda interacts with the memory control 108 (Kunda) so it is inherent that the cache know how much data (i.e. a full cache line in this case) is returning from main memory 109 via –sharing—of the information contained in the burst length register 212 of the memory control. Further it is necessarily inherent that this process occur so that cache always receive valid data from the main memory (in other words the cache would not receive 4 words and it was expecting 8 words). The examiner is considering the –address information— received to the cache controller (240 of Gaskins) to be the ADDR lines of figure 3. As can be seen by figures 3 and 5, the address lines contain address information regarding the first address of the burst and then, since the data processing device of Kunda can receive address data starting from the address in the cache line that caused the miss as described above, the cache control can then accept the data returned from the memory such as shown on the data lines in figure 5 of Gaskins. The examiner is further considering the –synchronization—signal received by the cache control (240 of Gaskins) to be the ADS# signal since valid data is returned in sync to when the ADS# signal transitions from logic 0 to logic 1. The examiner is

considering the cache fill address to be the address of the cache line where the data returned from the main memory is to be stored (i.e. lines 262 in figure 2 of Gaskins, for example).

Claims 3,8,11, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kunda et al. (U.S. Patent No. 5,715,476) in view of Gaskins et al. (U.S. Patent No. 6,081,853) in further view of Kobayashi et al. (U.S. Patent No. 5,394,528).

Kobayashi teaches a bus-sizing function that allows a processor to issue a single bus request instead of multiple requests over smaller external buses (column 7, lines 15-27) when data is to be accessed from main memory, such as in the event of a cache miss (column 3, line 37-39). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the data processing system of Kunda (with cache system represented by Gaskins) with the teaching of the bus-sizing function of Kobayashi in order to have reduced the complexity of the processor in the data processing system by eliminating the need for the internal function circuit of the processor to operate under the control of different procedures for different bus width sizes (column 7, lines 22-26).

As discussed in column 12, lines 17-23 of Kobayashi, a first burst access from a main memory in response to a cache miss (mishit) is accessed in order according to the block address causing the miss (in this case block address x0008) and then wrapping-around the address bounds for the burst, as can be seen by the transition from address x000C to x0000 (column 12, line 20). For a second burst transfer, accessing is performed in linear order starting with the --top boundary-- as can be seen in column 12, line 22.

***Conclusion***

Prior art made of record and not relied upon and considered pertinent to applicant's disclosure are listed in PTO-892.

Strongin et al. (U.S. Patent No. 6,185,637) teaches assigning burst lengths based on address ranges and latency.

Ryan et al. (U.S. Patent No. 6,405,280) teaches a cache line burst policy supporting a plurality of data orderings with a main memory comprising multiple memory modules.

Shaw (U.S. Patent No. 6,574,707) teaches a wrap-around access for the first burst and linear access for the following successive bursts.

Any inquiry concerning this communication or earlier communications from the xaminer should be directed to Shane M Thomas whose telephone number is (703) 605-0725. The examiner can normally be reached on M-F 8:30 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt M Kim can be reached on (703) 305-3821. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 764-7239 for regular communications and (703) 764-7239 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Shane M. Thomas
November 12, 2003

MATTHEW KIM
SUPERVISORY PATENT EXAMINER
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